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A Hardware-Based Multi-Stage Dynamic Power Management Architecture for Autonomous Low-Light Operation

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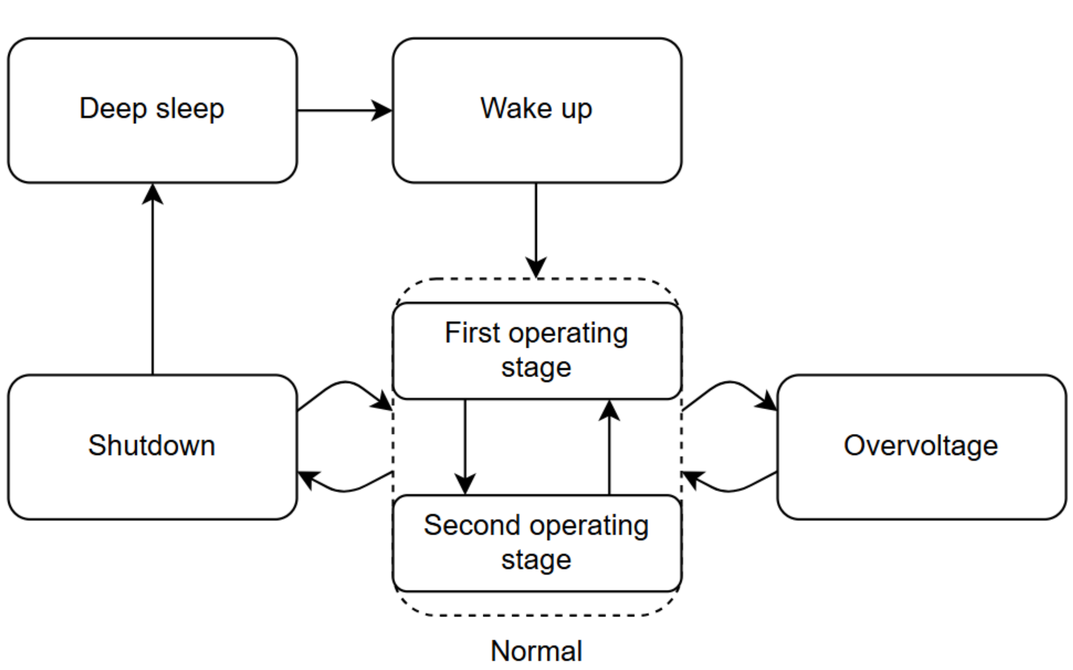
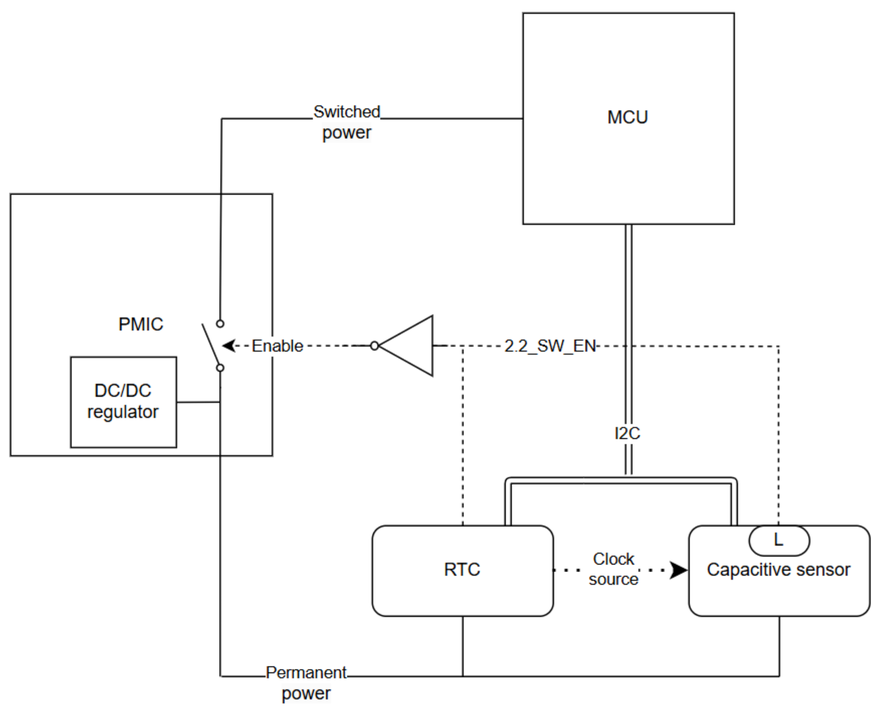
Background and Contribution

Dynamic Power Management (DPM) is essential for energy conservation.
Conventional software-based techniques that rely on processor-managed low-power states incur a persistent quiescent current drain.
We introduce a new hardware-orchestrated DPM architecture that achieves a minimal quiescent drain of $452nA$.
The MCU and all non-essential peripherals are power-gated, with wake-up orchestrated by an ultra-low-power PMIC, RTC and a novel latch circuit.





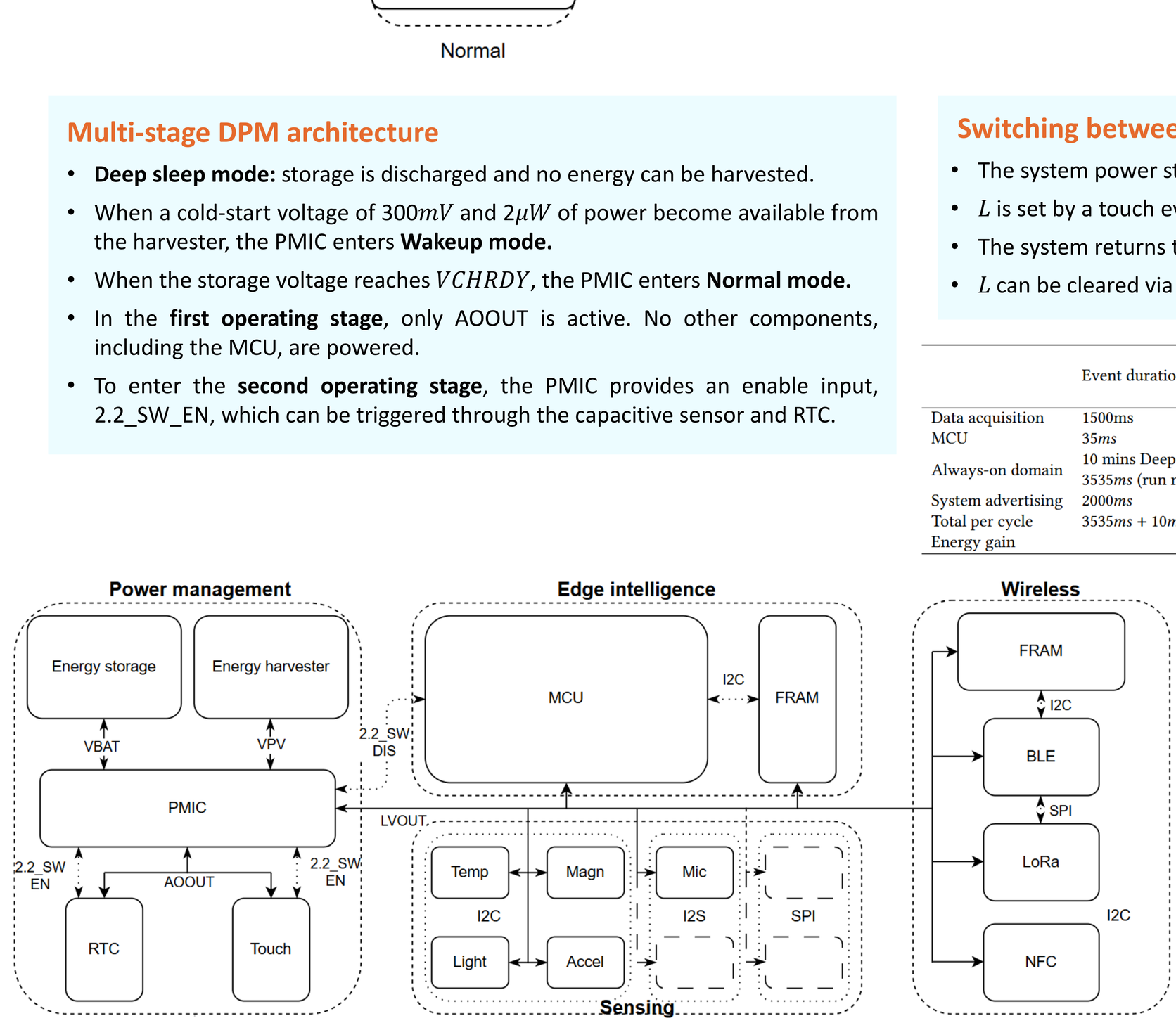
Multi-stage DPM architecture

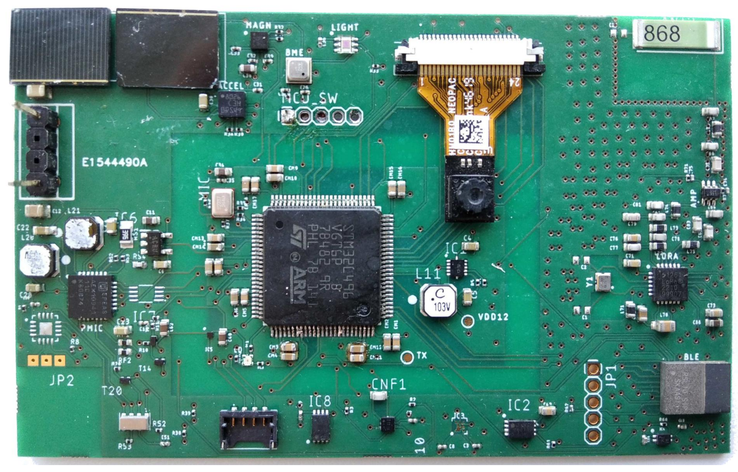
- **Deep sleep mode:** storage is discharged and no energy can be harvested.
- When a cold-start voltage of $300mV$ and $2\mu W$ of power become available from the harvester, the PMIC enters **Wakeup mode.**
- When the storage voltage reaches $VCHRDY$, the PMIC enters **Normal mode.**
- In the **first operating stage**, only AOOUT is active. No other components, including the MCU, are powered.
- To enter the **second operating stage**, the PMIC provides an enable input, 2.2_SW_EN, which can be triggered through the capacitive sensor and RTC.

Switching between operating stages

- The system power state is kept in internal latch L.
- L is set by a touch event or when the RTC pulls the signal 2.2_SW_EN low.
- The system returns to *deep sleep mode* by clearing L in the touch sensor.
- L can be cleared via an I²C command or a digital signal through 2.2_SW_DIS.

	Event duration	Energy required	Energy harvested under 200 lux for 10 minutes	Energy harvested under 300 lux for 10 minutes	Energy harvested under 500 lux for 10 minutes
Data acquisition	1500ms	$1.1mJ$			
MCU	$35ms$	$46.2\mu J$			
Always-on domain	10 mins Deep Sleep + $3535ms$ (run mode)	$0.6mJ$	$26.04mJ$	$38.2mJ$	$72.42mJ$
System advertising	$2000ms$	$0.4mJ$			
Total per cycle	$3535ms$ + $10min$	$2.14mJ$			
Energy gain			$23.9mJ$	$36.06mJ$	$70.28mJ$





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